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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO
09/602,474	06/23/2000	Joseph Herbst	108339-09036	1343
32294 75	590 09/30/2004		EXAM	INER
SQUIRE, SANDERS & DEMPSEY L.L.P.			LI, ZHUO H	
14TH FLOOR 8000 TOWERS CRESCENT			ART UNIT	PAPER NUMBER
	NER, VA 22182		2186	
			DATE MAILED: 09/30/200	4

Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)				
	09/602,474	HERBST, JOSEPH				
Office Action Summary	Examiner	Art Unit				
	Zhuo H Li	2186				
The MAILING DATE of this communication Period for Reply	appears on the cover sheet w	ith the correspondence address				
A SHORTENED STATUTORY PERIOD FOR RITHE MAILING DATE OF THIS COMMUNICATION. Extensions of time may be available under the provisions of 37 CF after SIX (6) MONTHS from the mailing date of this communication of the period for reply specified above is less than thirty (30) days, for NO period for reply is specified above, the maximum statutory provided to the second of the second	ON. R 1.136(a). In no event, however, may a r n. a reply within the statutory minimum of thirl eriod will apply and will expire SIX (6) MON statute, cause the application to become AE	eply be timely filed by (30) days will be considered timely. ITHS from the mailing date of this communication. BANDONED (35 U.S.C. § 133).				
Status						
1) Responsive to communication(s) filed on 2	26 July 2004.					
2a) ☐ This action is FINAL . 2b) ☑	This action is non-final.					
	Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under <i>Ex parte Quayle</i> , 1935 C.D. 11, 453 O.G. 213.					
Disposition of Claims						
4) ☐ Claim(s) 1-4 and 6-20 is/are pending in the 4a) Of the above claim(s) is/are with 5) ☐ Claim(s) is/are allowed. 6) ☐ Claim(s) 1-4 and 6-20 is/are rejected. 7) ☐ Claim(s) is/are objected to. 8) ☐ Claim(s) are subject to restriction as	ndrawn from consideration.					
Application Papers		and the second s				
9) The specification is objected to by the Examiner.						
10) The drawing(s) filed on is/are: a) accepted or b) objected to by the Examiner.						
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).						
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d). 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.						
Priority under 35 U.S.C. § 119	•					
12) Acknowledgment is made of a claim for form a) All b) Some * c) None of: 1. Certified copies of the priority docum 2. Certified copies of the priority docum 3. Copies of the certified copies of the application from the International But * See the attached detailed Office action for a	nents have been received. nents have been received in A priority documents have been reau (PCT Rule 17.2(a)).	pplication No received in this National Stage				
Attachment(s)						
1) X Notice of References Cited (PTO-892) 。 2)		ummary (PTO-413) s)/Mail Date,				
2) Information Disclosure Statement(s) (PTO-1449 or PTO/SE Paper No(s)/Mail Date	,	formal Patent Application (PTO-152)				

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DETAILED ACTION

Election/Restrictions

1. Applicant's election with traverse of the invention elected in the reply filed on 7/1/2004 is acknowledged. The traversal is on the ground(s) that the requirement for restriction in this application is improper. This is found persuasive. Thus, the previous Office action of June 1, 2004 is vacated. As a result, claims 1-4 and 6-20 are pending for examination.

Claim Rejections - 35 USC § 103

- 2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:
 - (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
- 3. Claims 1-4 and 6-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over McAllister et al. (US PAT. 6,501,755 hereinafter McAllister) in view of Hine (US PAT. 5,652,864).

Regarding claim 1, McAllister discloses a method for managing memoryin a network switch (220, figure 4) comprising the steps of providing a memory, i.e., address space, including a plurality of memory locations configured to store data, i.e., network message, therein (col. 9 lines 22-41), providing a memory address pool, i.e., address stack (224A, figure 4), having a plurality of available memory addresses arranged therein (col. 9 lines 47-55), wherein each of the

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plurality of memory addresses obviously corresponds to a specific memory location, and providing means for indicating a next available memory address in the memory address in order to perform push or read operation (col. 19 lines 18-23), wherein the method further comprises the steps of reading available memory addresses from the memory address pool using a last in first out operation (col. 19 lines 23-26), writing released memory addresses into the memory address pool (col. 19 lines 26-40), and adjusting a position of the memory address pointer upon a read or a write operation from the memory address pool when a release of a released memory address does not occur in a same clock cycle as a request for an available address (col. 19 line 41 through col. 20 line 8). McAllister differs from the claimed invention in not specifically teaching to pass off the released memory address in place of the available memory address when the release of the released memory address occurs in the same clock cycle as the request for the available address. However, Hine teaches a method for allocating storage blocks by concurrently allocating two or more storage requests capable of passing off a released memory address in place of an available memory address when the release of the released memory address occurs in the same clock cycle as the request for the available address in order to speed up the memory management operation by allocation or return request concurrently (col. 7 line 30 through col. 8 line 34). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify McAllister in passing off the released memory address in place of the available memory address when the release of the released memory address occurs in the same clock cycle as the request for the available address, as per teaching of Hine, because it speeds up the memory management operation by allocation or return request concurrently.

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Regarding claim 2, Hine teaches to initiate the steps of reading available memory addresses and writing released memory address during a second clock cycle when the reading step and the writing step are requested in a first clock cycle (col. 3 line 37 through col. 4 line 3).

Regarding claim 3, McAllister discloses a method for managing memory in a network switch (220, figure 4) comprising the steps of receiving a request from a module for a next available memory address in a first clock cycle and receiving a released memory address in the first clock cycle (col. 18 line 64 through col. 20 line 8). McAllister differs from the claimed invention in not specifically teaching the step of passing off the release memory address to the module requesting the next available memory address in place of the next available memory address in a second clock cycle, which is next clock cycle after the first clock cycle. However, Hine teaches a method for allocating storage blocks by concurrently allocating two or more storage requests capable of passing off a released memory address in place of an available memory address in a second clock cycle after the first clock cycle in order to speed up the memory management operation by allocation or return request concurrently (col. 7 line 30 through col. 8 line 34). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify McAllister in passing off the release memory address to the module requesting the next available memory address in place of the next available memory address in a second clock cycle, which is next clock cycle after the first clock cycle, as per teaching of Hine, because it speeds up the memory management operation by allocation or return request concurrently.

Regarding claim 4, Hine teaches to operate the passing off steps without incrementing or decrementing a next available memory address pointer associated with the memory (col. 8 lines 1-9).

Regarding claim 6, the limitation of the claim are rejected as the same reasons set forth in claim 1.

Regarding claim 7, the limitation of the claim are rejected as the same reasons set forth in claim 4.

Regarding claim 8, the limitation of the claim are rejected as the same reasons set forth in claim 1.

Regarding claims 9-10, McAllister discloses the memory address pool for storing and transporting data within intermediate networks (col. 9 ;ones 47-55) so that it recognizes the memory address pool comprises a cell free address pool or a slot free address pool.

Regarding claims 11-12, Hine teaches the memory controller being configured to read an available memory address form the memory address pool and to write a released memory address to the address pool and passing off the released memory address upon a request for the available memory address in the same clock cycle, i.e., concurrently, without adjusting the address pointer (col. 7 line 30 through col. 8 line 34).

Regarding claim 13, the limitation of the claim are rejected as the same reasons set forth in claim 1.

Regarding claims 14-15, Hine discloses the memory or storage in the form of RAM (col. 2 lines 65-66) so that one skill in the art would recognize the memory also comprising SRAM or SDRAM in order to make compatibility with different memories.

Regarding claims 16-17, the limitations of the claims are rejected as the same reasons set forth in claim 9-10.

Regarding claims 18-19, Hine discloses the memory controller comprising a common buffer pool controller or SDRAM controller (col. 2 line 64 through col. 3 line 10).

Regarding claim 20, the limitation of the claim are rejected as the same reasons set forth in claim 1.

Response to Arguments

4. Applicant's arguments with respect to claims 1-4 and 6-20 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

- 5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Hughes (US PAT. 5,784,582) discloses a data processing system having a memory controller for supplying current request and next request for accessing a memory (abstract).
- 6. Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

Or faxed to:

(703) 308-6606

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Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive,

Arlington, VA, Fourth Floor (Receptionist).

7. Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Zhuo H. Li whose telephone number is 703-305-3846. The

examiner can normally be reached on Tuesday to Friday from 9:30 a.m. to 7:00 p.m. The

examiner can also be reached on alternate Monday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Matthew Kim, can be reached on (703) 305-3821.

Any inquiry of a general nature or relating to the status of this application or proceeding

should be directed to the receptionist whose telephone number is (703) 305-3900.

Zhuo H. Li

Árt Unit 2186

MATTHEW KINT

PERVISORY PATENT EXAMINER

MOLOGY CENTER 2100